Gate Tangchartsiri

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Education

Georgia Institute of Technology Atlanta, GA
Bachelor of Science in Computer Engineering, GPA: 3.72/4.00 *August 2022 – May 2026*
Concentrations: Computing Hardware and Distributed Systems

Technical Skills

Languages: C, Verilog, SystemVerilog, VHDL, Python, CUDA, Triton, Java, ARM, RISC-V, MIPS, TCL
Developer Tools: Cadence Virtuoso, Cadence Innovus, Verilator, Icarus Verilog, PyTorch, GTKwave, Git, Docker
Infrastructure: Linux, Bash, Makefiles
Communication Protocols: PCIe (LTSSM), I2C, SPI, Ethernet, BLE, UART
Coursework: Advanced Computer Architecture, HW/SW Co-Design, GPU Programming, Advanced VLSI Design

Work Experiences

Physical Design Engineer January 2025 – Present
SiliconJackets *Atlanta, GA*

- Resolved Caravel harness DRC violations in the Sky130 PDK through layout modifications in Cadence Virtuoso, ensuring successful five-stage pipeline and superscalar tapeouts.
- Built PipeOpt, a Python CLI tool that analyzes Cadence Innovus static timing analysis (STA) reports and applies ILP-based optimization to automate register insertion decisions, eliminating manual timing review.

Product Applications Engineer Intern May 2025 – August 2025
Astera Labs *San Jose, CA*

- Verified PCIe retimer firmware behavior by probing intermediate signals on a logic analyzer, identifying signal timing violations.
- Designed a PCIe retimer bit error rate (BERT) demonstration for customers, showcasing retimer signal regeneration and diagnostics capabilities.
- Validated PCIe pseudorandom binary sequence (PRBS) pattern generation across the connectivity management platform, expanding automated link quality testing.

Research Project Lead January 2023 – May 2024
Georgia Institute of Technology *Atlanta, GA*

- Led a team of 10 engineering students to develop a SaaS dashboard for visualizing machine maintenance data from the Georgia Tech Flowers Invention Studio.
- Architected a Teensy-to-AWS RDS IoT pipeline for real-time band saw vibration and power usage data collection using MQTT and AWS IoT Core.

Projects

PipeOpt - ILP-Driven Register Insertion Optimizer | *STA, ILP, Cadence Innovus* January 2026 – Present

- Engineered a Python CLI tool that parses static timing analysis (STA) reports and netlists from Cadence Innovus, enabling the mapping of post-signoff paths to RTL hierarchy.
- Formulated the register insertion problem as a PuLP-based binary integer linear program, balancing delay budget constraints against register insertion count.
- Eliminated manual STA report reviewing process, reducing the timing analysis to a single CLI command.

Bike Buddy - Embedded Sensor Suite for Bike Maintenance | *C/C++* August 2025 – December 2025

- Implemented ESP32 Bluetooth firmware for the onboard sensor suite and companion mobile app, enabling real-time predictive wheel wobble and brake wear detection.
- Fabricated a laser-cut wheel mount for the non-invasive tracking of odometry and braking data.
- Awarded Best ECE Project, Georgia Institute of Technology, Design Capstone Expo Fall 2025.